

PATENT

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES**

In re Application of:

James M. Derderian

Serial No.: 09/939,258

Filed: August 24, 2001

For: SEMICONDUCTOR DEVICES
INCLUDING STACKING SPACERS
THEREON, ASSEMBLIES INCLUDING
THE SEMICONDUCTOR DEVICES, AND
METHODS

Confirmation No.: 2185

Examiner: D. Graybill

Group Art Unit: 2894

Attorney Docket No.: 2269-4831US

VIA ELECTRONIC FILING
October 28, 2008

REPLY BRIEF

Mail Stop Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Attn: Board of Patent Appeals and Interferences

Sirs:

This Reply Brief is being submitted within two months of the date on which an
Examiner's Answer was mailed in the above-referenced appeal and pursuant
to 37 C.F.R. § 41.41.

(7) ARGUMENT

The Examiner has gone to great lengths to support his assertion that the term “back side” in independent claims 1 and 18 should be very broadly construed to include any surface of a semiconductor device. Although the Examiner has apparently quoted M.P.E.P. § 2111.01 in its entirety, he has apparently overlooked the portion of section 2111.01 that provides:

[T]he ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, i.e., as of the effective filing date of the patent application.”
Phillips v. AWH Corp., >415 F.3d 1303, 1313<, 75 USPQ2d 1321>, 1326< (Fed. Cir. 2005) (en banc). ...

M.P.E.P. § 2111.01(III).

It is well known to those of ordinary skill in the art that a semiconductor die or wafer (or other fabrication substrate) includes an “active surface” upon which integrated circuitry is fabricated and an opposite “back side.” In fact, these terms have long been used throughout the patent literature. A recent search for the terms “back side” and “semiconductor” in the abstracts of U.S. Patents that had issued as of October 28, 2008, returned 460 results. Three of those patents were examined by the same Examiner to whom this application has been assigned. As an example of those results, U.S. Patent 6,828,175 to Wood et al. (hereinafter “Wood”) (which was filed after the above-referenced application, but illustrates that those of ordinary skill in the art know the meaning of the term “back side”) clearly explains that a semiconductor die includes two sides: one side that bears circuits and an opposite, “back side.” *See, e.g.*, col. 2, lines 62-64. This meaning of the term “back side” is supported by U.S. Patent 6,096,568 to Dobrovolski, which, at col. 4, lines 16-29, explains that the “back side” of a die is the surface from which material may be removed in thinning (*i.e.*, back grinding or milling) processes. In view of the

foregoing, it is respectfully submitted that the meaning of the term “back side” would have been apparent to one of ordinary skill in the art at the time the above-referenced application was filed.

In rejecting claims 1, 5-8, 10-23, 25, 28, 30-35, 53, and 54, the Examiner has relied upon two references (Hikita and Eldridge) with teachings that are limited to assemblies in which the active surfaces of two semiconductor devices face each other. The active surface-to-active surface arrangements of Hikita and Eldridge are necessary to electrically connect the assembled semiconductor device to each other in the manner disclosed by those references—assemblies in which the back side of one semiconductor device faces the active surface of another semiconductor device would not be useful in the assemblies of Hikita or Eldridge.

As neither Hikita nor Eldridge teaches or suggests an assembly in which the back side of one semiconductor device faces the active surface of another semiconductor device, neither Hikita nor Eldridge teaches or suggests an assembly in which at least one spacer “defines a distance the active surface of... at least one semiconductor device is to be spaced apart from a back side of another semiconductor device,” as recited by independent claim 1. Moreover, neither Hikita nor Eldridge teaches or suggests an assembly in which laterally spaced discrete spacers protrude from an active surface of one semiconductor device, and a back side of another semiconductor device is positioned on the spacers. It is, therefore, respectfully submitted that a *prima facie* case of obviousness has not been established against independent claim 1, independent claim 18, or any of their dependent claims.

Pu does not remedy the deficiencies of Hikita and Eldridge.

Accordingly, reversal of the 35 U.S.C. § 103(a) rejections of claims 1, 5-8, 10-23, 25, 28, 30-35, 53, and 54 is respectfully solicited, as is the allowance of each of these claims.

(11) CONCLUSION

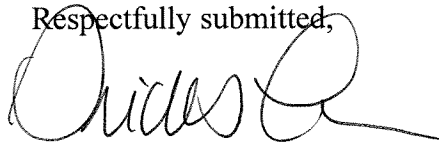
It is respectfully submitted that:

(A) Claims 1, 5-8, 10-23, 25, 28, 31, 32, 34, 35, 53, and 54 are each allowable under 35 U.S.C. § 103(a) for reciting subject matter that patentable over the teachings of Hikita and Eldridge; and

(B) Claims 16, 30, and 33 are allowable under 35 U.S.C. § 103(a) for being drawn to subject matter that is patentable over the subject matter taught in Hikita, Eldridge, and Pu.

Accordingly, it is respectfully requested that the 35 U.S.C. § 103(a) rejections of claims 1, 5-8, 10-23, 25, 28, 30-35, 53, and 54 be reversed, and that each of claims 1, 5-25, 28-35, 53, and 54 be allowed.

Respectfully submitted,



Brick G. Power
Registration No. 38,581
Attorney for Applicant
TRASKBRITT, PC
P.O. Box 2550
Salt Lake City, Utah 84110-2550
Telephone: 801-532-1922

Date: October 28, 2008
BGP/ec
Document in ProLaw